

Roll No.

MCA–05/PGDCA–05/M. Sc.(IT)–05

Computer Organization and Architecture

Master of Computer Applications/P. G. Diploma in
Computer Applications/Master of Science in
Information Technology
(MCA–11/16, PGDCA–11/16, M. Sc.(IT)–12/16)
Second Semester, Examination, 2017

Time : 3 Hours

Max. Marks : 70

Note : This paper is of **seventy (70)** marks containing **three (03)** sections A, B and C. Attempt the questions contained in these sections according to the detailed instructions given therein.

Section–A

(Long Answer Type Questions)

Note : Section ‘A’ contains four (04) long answer type questions of fifteen (15) marks each. Learners are required to answer *two* (02) questions only.

1. Answer the following :
 - (a) Define addressing mode and explain the basic addressing modes with an example for each.
 - (b) Explain how the virtual address is converted into real address in a paged virtual memory system.
2. Answer the following :
 - (a) How data transfer can be controlled using handshaking technique ?

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- (b) What are the different secondary storage devices ? Elaborate on any *one* of the devices.
3. Answer the following :
- (a) How interrupt request from different devices can be handled ?
- (b) How many memory chips are needed to construct $2\text{ M} \times 16$ memory system using $512\text{ K} \times 8$ static memory chips ?
4. Answer the following :
- (a) What are the needs for input-output interface ? Explain the function of a typical 8-bit parallel interface in detail.
- (b) State the hardware needed to implement the LRU in replacement algorithm.

Section-B

(Short Answer Type Questions)

Note : Section 'B' contains eight (08) short answer type questions of five (5) marks each. Learners are required to answer *six* (06) questions only.

1. Answer the following :
- (a) List and explain the steps involved in the execution of a complete instruction.
- (b) Under what situations the micro program counter is not incremented after a new instruction is fetched from micro program memory ?

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2. Explain different types of mapping functions in cache memory.
3. What is TLB (Translation Look Aside Buffer) ? What are its functions ?
4. Define locality of reference. What are its types ?
5. Explain micro-programmed control unit. What are its advantages and disadvantages ?
6. What is an opcode ? How many bits are used to specify 32 distinct operations ?
7. Compare RISC with CISC architecture.
8. What are the advantages and disadvantages of hardwired and microprogrammed control unit ?

Section-C

(Objective Type Questions)

Note : Section 'C' contains ten (10) objective type questions of one (1) mark each. All the questions of this section are compulsory.

1. The average time required to reach a storage location in memory and obtain its contents is called the :
 - (a) Seek time
 - (b) Turnaround time
 - (c) Access time
 - (d) Transfer time
2. Which of the following is not a weighted code ?
 - (a) Decimal Number system
 - (b) Excess 3-code
 - (c) Binary number system
 - (d) None of these

3. The idea of cache memory is based :
 - (a) On the property of locality of reference
 - (b) On the heuristic 90-10 rule
 - (c) On the fact that reference generally tend to cluster
 - (d) All of the above
4. Which of the following is lowest in memory hierarchy ?
 - (a) Cache memory
 - (b) Secondary memory
 - (c) Registers
 - (d) RAM
5. The addressing mode used in an instruction of the form ADD X Y, is :
 - (a) Absolute
 - (b) Indirect
 - (c) Index
 - (d) None of these
6. If memory access takes 20 ns with cache and 110 ns with out it, then the ratio (cache uses a 10 ns memory) is :
 - (a) 93%
 - (b) 90%
 - (c) 88%
 - (d) 87%

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7. In a memory-mapped I/O system, which of the following will not be there ?
 - (a) LDA
 - (b) IN
 - (c) ADD
 - (d) OUT
8. In a vectored interrupt :
 - (a) The branch address is assigned to a fixed location in memory
 - (b) The interrupting source supplies the branch information to the processor through an interrupt vector
 - (c) The branch address is obtained from a register in the processor
 - (d) None of the above
9. Von Neumann architecture is :
 - (a) SISD
 - (b) SIMD
 - (c) MIMD
 - (d) MISD
10. The circuit used to store one bit of data is known as :
 - (a) Encoder
 - (b) OR gate
 - (c) Flip Flop
 - (d) Decoder

